WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

an execution engine clocked at a first clock rate;

a memory controller clocked at a second clock rate less than the first clock rate; and

a plurality of pins adapted to transfer data to and from the memory controller on both the rising and falling edges of a second clock signal transitioning at the second clock rate.

2. The integrated circuit as recited in claim 1, further comprising a multiplexer coupled to receive a first clock signal that transitions at the first clock rate and the second clock that transitions at the second clock rate.

3. The integrated circuit as recited in claim 2, wherein the multiplexer is coupled to send the second clock signal to the memory controller during times when the memory controller receives a power supply voltage.

4. The integrated circuit as recited in claim 1, wherein the memory controller is adapted to produce both a true and complementary said second clock signal on a pair of output pins of the integrated circuit.

5. The integrated circuit as recited in claim 1, wherein the plurality of pins are adapted to transfer data faster than the first clock rate.

6. The integrated circuit as recited in claim 1, further comprising:

a configuration register adapted to store a logic value;

a multiplexer; and

a latch having an input coupled to the configuration register and an output coupled to a select input of the multiplexer for selecting the second clock signal in lieu of a first clock signal depending on a logic voltage value stored within the configuration register.

7. The integrated circuit as recited in claim 1, wherein the memory controller is coupled to receive a power supply voltage less than 2.5 volts.

8. The integrated circuit as recited in claim 1, wherein the integrated circuit comprises a plurality of bonding pads wire bonded to corresponding leads emanating from the integrated circuit.

9. An electronic system, comprising:

a substrate comprising a maximum or two conductive layers spaced from each other by a dielectric layer;

an execution engine electrically coupled to a first conductor extending partially across one of the two conductive layers, wherein the execution engine is adapted to receive a first clock signal which cycles at a first clock rate;

a memory controller electrically coupled to a second conductor extending partially across one of the two conductive layers, wherein the memory controller is adapted to receive a second clock signal which cycles at a second clock rate less than the first clock rate;

a memory device electrically coupled to a third conductor extending partially across one of the two conductive layers, wherein the memory device comprises an array of dynamic random access memory cells; and

a data bus extending partially across one of the two conductive layers and between the memory controller and the memory device, wherein the data bus is adapted to transfer data at a rate greater than the first clock rate and at substantially twice the second clock rate.

10. The electronic system as recited in claim 9, wherein one of the two conductive layers resides on an outer surface of the substrate.

11. The electronic system as recited in claim 9, wherein the execution engine, the memory controller and the memory device comprises a packaged integrated circuit having a plurality of leads extending therefrom.

12. The electronic system as recited in claim 11, wherein each said execution engine, said memory controller and said memory device comprise bonding pads and a leadframe having bonding fingers that extend to a plurality of respective leads, and wherein a wire is solder coupled between a respective pair of bonding pads and bonding fingers.

13. The electronic system as recited in claim 11, wherein one of the two conductive layers comprises a set of solder pads to which the plurality of leads are solder coupled.

14. The electronic system as recited in claim 9, wherein the execution engine, the memory controller and the memory device are mounted on an outer surface of the substrate.

15. The electronic system as recited in claim 9, wherein the two conductive layers comprises a plurality of laterally spaced conductors comprising copper.

16. The electronic system as recited in claim 9, wherein the dielectric layer comprises epoxy-bonded fiberglass.

17. The electronic system as recited in claim 15, wherein at least one conductor within a first one of the two conductive layers is coupled by a conductive via to at least one conductor within a second one of the two conductive layers.

18. The electronic system as recited in claim 9, wherein the terminal ends of the data bus are terminated through pull-up resistors and output drivers connected to a reference supply less than 2.5 volts.

19. The electronic system as recited in claim 18, wherein the pull-up resistors and output drivers comprise termination devices for connecting ends of the plurality of primary and secondary conductors according to stub series terminated logic (SSTL).

20. The computer as recited in claim 11, wherein the execution engine and the memory controller are embodied upon a first integrated circuit separate and apart from the memory device embodied upon a second integrated circuit, and wherein both the first and second integrated circuits are packaged in separate thin small outline packages (TSOPs) with leads extending from the each TSOP to corresponding solder pads upon the substrate.

21. A method for transferring data between a memory controller and a memory device, comprising:

integrating an execution engine with a memory controller;

clocking the execution engine with a first clock that cycles at a first clock rate;

clocking the memory controller with a second clock that cycles at a second clock rate less than the first clock rate;

clocking a memory device, formed separate and apart from the integrated execution engine and memory controller, with the second clock; and

transferring data between the memory controller and the memory device at both the leading and trailing edges of the second clock.

22. The method as recited in claim 21, further comprising:

packaging the integrated execution engine and memory controller;

packaging the memory device;

coupling the packaged integrated execution engine and memory controller to a printed circuit board;

coupling the packaged memory device to the printed circuit board; and

wherein the printed circuit board comprises a plurality of conductors arranged within a maximum of two conductive layers spaced from each other by a dielectric layer.

23. The method as recited in claim 22, further comprising terminating opposing first and second ends of each of said plurality of conductors that accommodates the transfer of data with a pull-up resistor to a power supply having a voltage value dissimilar from a voltage value placed on the memory device, and wherein the voltage value placed on the pull-up resistor is less than 2.5 volts.

24. The method as recited in claim 22, further comprising terminating opposing first and second ends of each of said plurality of conductors according to stub series terminated logic (SSTL).